Ordering number : ENA1003

SANYO Semiconductors
DATA SHEET

LV24030LP — Bi-CMOS IC
FM Tuner IC for Small Portable Equipment

Overview

The LV24030LP is FM tuner IC's that requires absolutely no external components for tuning.
They incorporates not only the FM tuner functions as well in a compact VQLP package with dimensions of only 4.0×4.0×0.8mm.
These IC's are simply ideal for incorporating FM tuner functions into mobile phones and other small mobile set where space is always at a premium.

Functions

- FM FE
- FM IF
- MPX stereo decoder
- Tuning
- Standby

Features

- No external components
- No alignments necessary
- Fully integrated low IF (140kHz) selectivity and demodulation
- Built in adjacent channel interface total reduction (no 114kHz, no 190kHz)
- Due to new tuning concept, the tuning is independent of the channel spacing
- Very high sensitivity due to integrated low noise RF input amplifier
- Very low power standby mode. No power switch circuitry required
- MPX output for RDS application
- 3-wire bus interface (Date, Clock, NR-W)
- Digital AFC-Tuner locks to frequency after tuning sequence
- 4 level programmable Soft Mute
- 4 level Programmable Stereo Blend

Continued on next page.

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Continued from preceding page.

- In combination with the host, fast, low power operation of present mode, manual search, automatic search and automatic present store are possible
- Covers all Japanese, European and US bands
- Built in voltage stabilizer
- Stereo pilot signal Canceller

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	Analog block supply voltage	5.0	V
	V_{DD} max	Digital block supply voltage	4.5	V
Digital input voltage	$V_{IN}1$ max	Clock, Data, NR_W	V_{DD}+0.3	V
	$V_{IN}2$ max	External_clk_in	V_{DD}+0.3	V
Allowable power dissipation	Pd max	Ta≤70°C, Mounted on a specified board *	140	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

Note: Mounted on a specified board: 40mm×50mm×0.8mm, glass epoxy

Operating Condition at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}	Analog block supply voltage	3.0	V
	V_{DD}	Digital block supply voltage	3.0	V
Operating supply voltage range	V_{CC} op		2.6 to 4.0	V
	V_{DD} op		2.5 to 4.0	V
	V_{IO} op	Interface voltage	1.8 to 4.0	V

Note: The V_{IO} application voltage must be either equivalent to V_{DD} or the V_{DD} value or less. ($V_{IO} \leq V_{DD}$)

Interface Block Allowable Operation Range at Ta = -20 to +70°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.5		4.0	V
Digital block input (including the external clock)	V_{IH}	High level input voltage range	0.7V_{IO}		V_{IO}	V
	V_{IL}	Low level input voltage range	0		0.6	V
Digital block output	I_{OL}	Output current at Low level	2.0			mA
	V_{OL}	Output voltage at Low level I_{OL}=2mA			0.6	V
Clock input operating frequency	fclk	(Pin5) clock frequency for 3wire_bus			0.7	MHz
External clock operating frequency	fclk_ext	(Pin12) clock frequency for external input	32k		20M	Hz

Note: External clock input (pin12) allows also input of the sine wave signal.

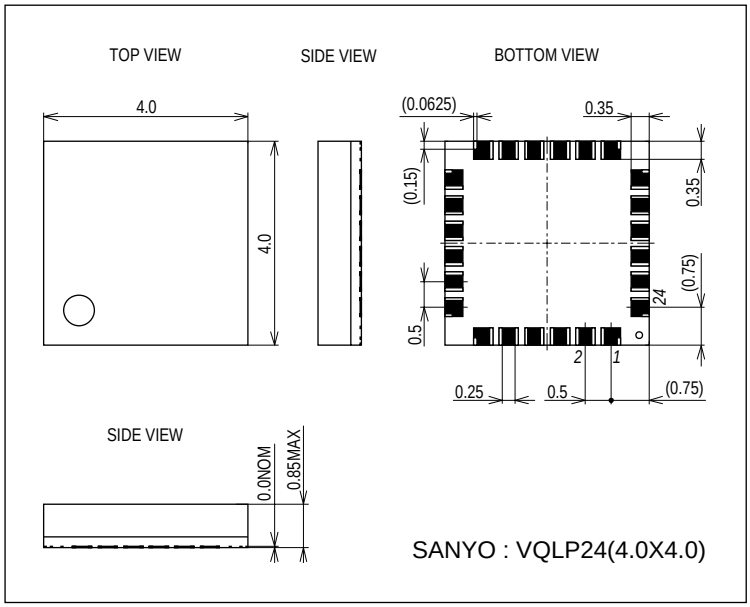
Operating Characteristics at Ta=25°C, V_{CC}=3.0V, V_{DD}=3.0V, Soft Mute/Soft Stereo=off, with the specified test circuit.

Output level setting is for the maximum output setting by setting Bit 4 and Bit 5 (Audio output level bits) of Address 04h of the control register map to "1" respectively. In other cases, the IF_BW set Bit value is when the value has been set to 65% of the IF_OSC set Bit value.
(Register setting for IF_OSC set =140kHz and IF_BW=140kHz*0.65)

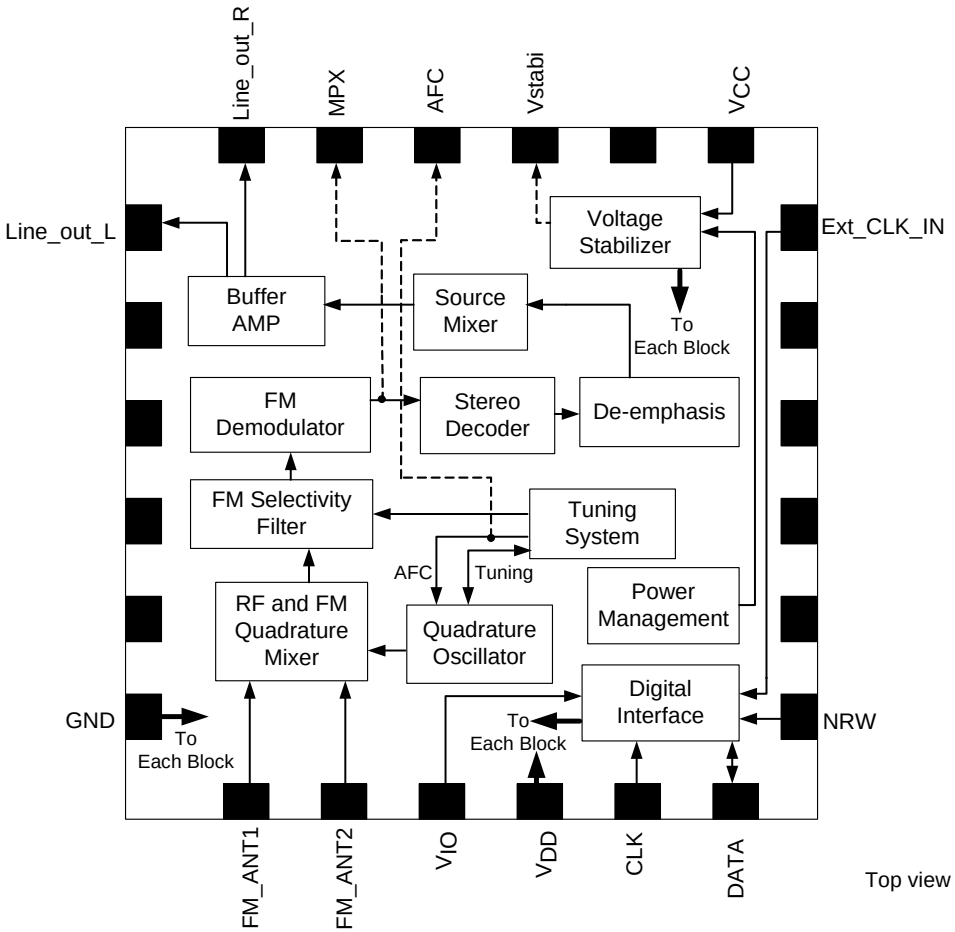
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain (in operation)	ICCA	Measurement at pin 13 with 60dBμ input in the analog block, Monaural input		12	17	mA
	ICCD	Measurement at pins 3 and 4 with 60dBμ input in the digital block		0.3	0.8	
Current drain (in standby)	ICCA	Measurement at pin 13 in the standby mode of the analog block		3	30	μA
	ICCD	Measurement at pins 3 and 4 in the standby mode of the digital block.		3	30	
FM receive band	F_range	When mounted to PCB with SANYO recommended conditions	76		108	MHz
FM receiving characteristics MONO : fc=80MHz, fm=1kHz, 22.5kHz dev. Note that Soft_stereo, Soft_and mute functions are OFF.						
3dB sensitivity	-3dB LS	60dBμV, 22.5kHz dev. output standard, -3dB input.		5	17	dBμV EMF
Practical sensitivity 1	QS1	Input level with S/N=30dB De-emphasis=75μs SG open display		8	16	dBμV
Practical sensitivity 2 (Reference)	QS2	Input level with S/N=26dB De-emphasis=75μs, SG terminal display		1.1		μV
Demodulator output	V_O	60dBμV, pin 18, pin 19 output	80	110	160	mV
Channel balance	CB	60dBμV, pin 18 / pin 19 output	-2	0	2	dB
Signal-to-noise ratio	S/N	60dBμV, pin 18, pin 19 output	48	58		dB
Total harmonic distortion 1 (MONO)	THD1	60dBμV, pin 18, pin 19 output, 22.5kH dev.		0.4	1.5	%
Total harmonic distortion 2 (MONO)	THD2	60dBμV, pin 18, pin 19 output, 75kH dev.		1.3	3.0	%
Field intensity display level	FS	Input level at which FS1 changes to FS2, Reg04_bit3=0	3	10	20	dBμ
Mute attenuation	Mute-Att	60dBμV, pin 18, pin 19 output	60	70		dB
FM receive characteristic STEREO characteristics : fc=80MHz, fm=1kHz, V_{IN}=60dBμV, Pilot=10%(7.5kHz dev.)						
Separation	SEP	L-mod, Pin19, pin18 output L+R signals =30%(22.5kHz dev.)	20	35		dB
Total harmonic distortion (Main)	THD-ST	Main-mod (for L+R input), Pin19, pin18 output IHF_BPF, L+R=30%(22.5kHz dev.)		0.6	1.8	%

Package Dimensions

unit : mm (typ)
3347

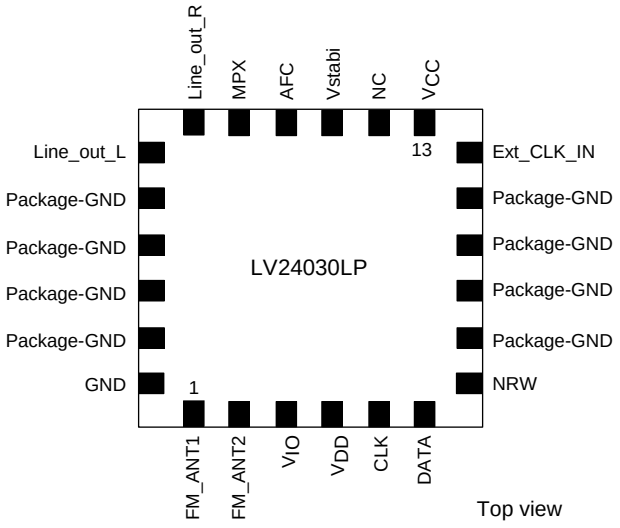


Block Diagram and Pin Assigment



Pin Discription

Pin	Name	Description	Remarks	DC_bias
1	FM-ANT1	Antenna input	FM signal input point	1V
2	FM-ANT2	Antenna GND	Connect to GND with capacitor	1V
3	VI/O	Digital interface supply voltage	Connect to power supply	
4	V_{DD}	Digital supply voltage	Connect to power supply	
5	CLOCK	Digital interface Clock	Control pin	
6	DATA	Digital interface DATA	Control pin	
7	NR_W	Digital interface Read/Write	Control pin	
8	Package-GND	GND for package-shield	Connect to GND	
9	Package-GND	GND for package-shield	Connect to GND	
10	Package-GND	GND for package-shield	Connect to GND	
11	Package-GND	GND for package-shield	Connect to GND	
12	Ext_CLK_IN	Reference clock-source input for measurement	Control pin Connect to GND if not used	
13	V_{CC}	Analog supply voltage	Connect to power supply	
14	NC		Open	
15	Vstabi.	Stabilizer voltage	Open	2.5V
16	AFC	AFC control bias	Put capacitor between 16 pin and GND Otherwise, open if not used	1.1
17	MPX	MPX-signal output	Open	2.3V
18	LINE-OUT-R	Radio Rch Line-output	Output pin	1V
19	LINE-OUT-L	Radio Lch Line-output	Output pin	1V
20	Package-GND	GND for package-shield	Connect to GND	
21	Package-GND	GND for package-shield	Connect to GND	
22	Package-GND	GND for package-shield	Connect to GND	
23	Package-GND	GND for package-shield	Connect to GND	
24	GND	GND (Analog and Digital GND)	Connect to GND	

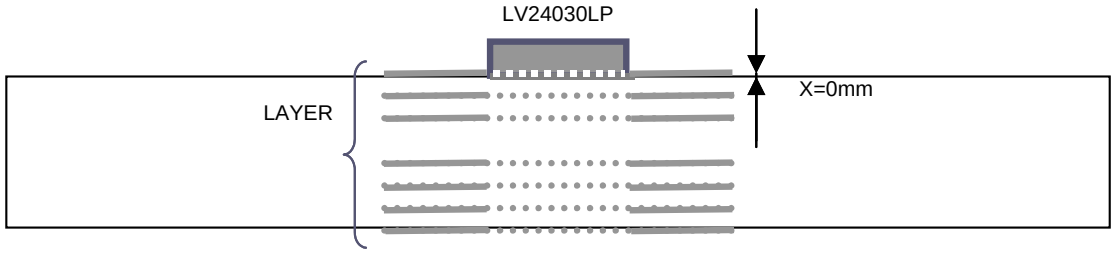


Top view

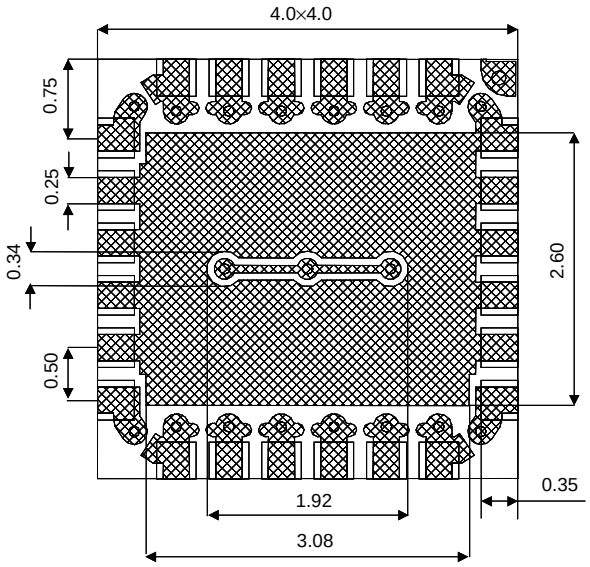
The PCB mounting conditions which cover FM receiving frequency range 76MHz to 108MHz

LV24030LP has an inductor for local oscillator on the package bottom side.
In order to cover the receiving frequency range of 76MHz to 108MHz, provide the GND layer to the first layer of Side A of PCB that is directly under the package bottom side, as shown in the figure.

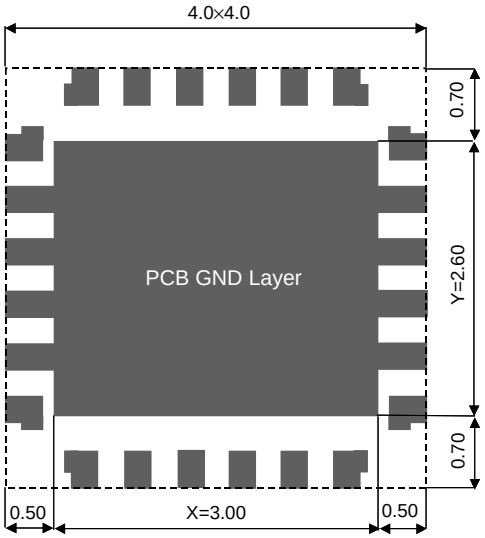
Printed circuit board



PCB layout recommendations



IC substrate LV24030LP

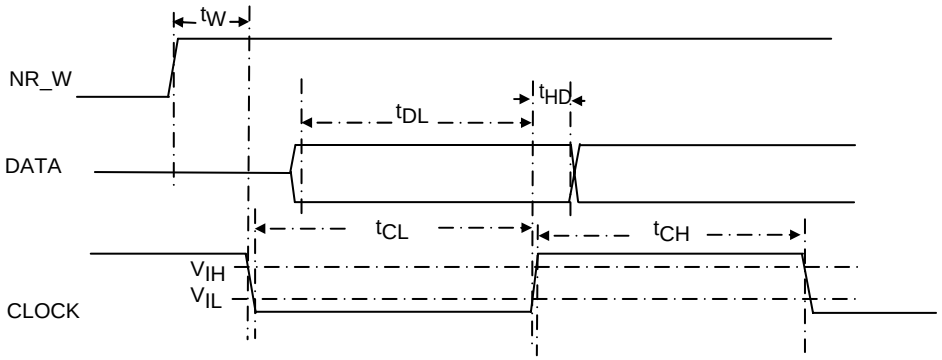


Recommended GND layer
for PCB substrate directly under IC

With this SPL, the receiving frequency is measured under the following conditions:
The X-value can be set freely between Min=2.4mm and Max=3.0mm with reference to IC.
(The X-value for SANYO Demo Board is 2.8mm.)
The Y-value can be set freely between Min=2.0mm and Max=3.0mm with reference to IC.
(The Y-value for SANYO Demo Board is 2.6mm.)
Avoid providing another wiring within 0.4mm of bottom layer of PCB_GND as much as possible.

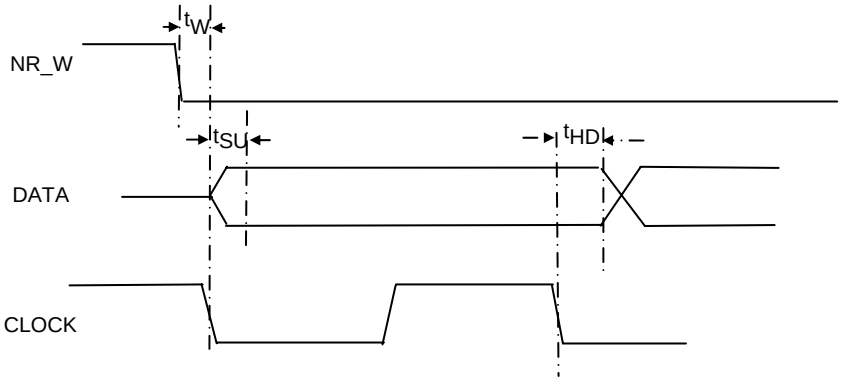
Serial Data Timing

• Write timing



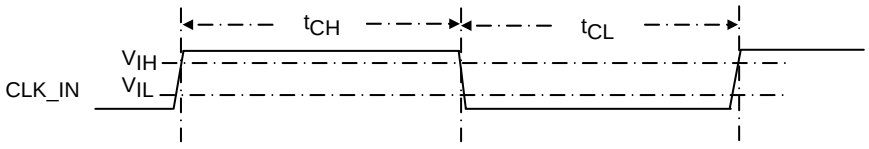
Symbol	Conditions	Ratings			Unit
		min	typ	max	
t_W	Delay from command to data	750			ns
t_{DL}	Delay from data stable to data latch time	750			ns
t_{HD}	Data Hold time	750			ns
t_{CH}	Clock High-level time	750			ns
t_{CL}	Clock Low-level time	750			ns

• Read timing



Symbol	Conditions	Ratings			Unit
		min	typ	max	
t_W	Delay from command to 1st data bit	350			ns
t_{SU}	Data Setup time			350	ns
T_{HD}	Data hold time			350	ns

• External clock timing (Pin 31)



Symbol	Conditions	Ratings			Unit
		min	typ	max	
t_{CH}	Clock High-level time	35			ns
t_{CL}	Clock Low-level time	35			ns

Digital Interface Specification (reference)

• 3-wire bus (For communication line)

Access to the LV24030 is done through the 3-wire bus.

CLOCK	Clock
NR_W	Write/read control
DATA	Data is written into LC24030 when the bidirectional communication line NR_W is H and is read from LV24030 when NR_W is L.

LV24030 has a function to notify occurrence of interruption by means of change in the DATA line.
If interruption is to be made, it is essential that the controller supports interruption by change of the DATA line.

When the timing necessary for frequency measurement cannot be generated from the controller, it is necessary to input the external clock (oscillator or 32kHz crystal) to the CLK_IN pin of LV24030.

• Register map

Address	Register name	Access	Operation
00h	CHIP_ID	R	Chip identification
01h	NA	-	
02h	CNT_L	R	Counter value low byte
03h	FM_OSC	W	DAC control for FM-RF oscillator
04h	AUDIO_CTRL	W	Audio Control
05h	MSRC_SEL	W	Measure source select
06h	CTRL_STAT	R	Control status
07h	RADIO_STAT	R	Radio station status
08h	STEREO_CTRL	W	Stereo Control
09h	FM_CAP	W	RM-RF CAP bank DAC setting
0Ah	PW_SCTRL	W	Power and soft control
0Bh	SD_OSC	W	DAC control for stereo decoder oscillator
0Ch	CNT_CTRL	W	Counter control
0Dh	CNT_STAT	R	Control status
0Eh	IF_OSC	W	DAC control for IF oscillator
0Fh	IF_BW	W	IF Bandwidth
10h	RADIO_CTRL1	W	Radio control 1
11h	CNT_H	R	Counter value high byte

Registers with blank colum are not defined and should not be accessed.

Register Description (For each resister content)

Register 00h-CHIP_ID-Chip Identify Register (Read only)

7	6	5	4	3	2	1	0
ID[7:0]							

Bit 7-0: **ID[7:0]**: 8-bit chip ID
LV24030:02h

Register 02h-CNT_L-Counter Value Low Register (Read-only)

7	6	5	4	3	2	1	0
CNT_LSB[7:0]							

Bit 7-0: **CNT_LSB[7:0]**: Lower 8-bit value of the 16 bit counter

Register 03h-FM_OSC-FM RF Oscillator Register (Write-only)

7	6	5	4	3	2	1	0
FMOSC[7:0]							

Bit 7-0: **FMOSC[7:0]**: DAC value to control the FM RF oscillator (fine step)

Register 04h – AUDIO_CTRL – Audio Control Register (Write-only)

7	6	5	4	3	2	1	0
Reserved		nVOL1	nVOL0	Reserved	DEEMP	AMUTE_L	SE_FM

Bit 7-6: **Reserved**: Fixed at 0
Bit 5-4: **nVOL[1:0]**: Audio output level
11b = Maximum output level
10b = Output level 3
01b = Output level 2
00b = Minimum output level
Bit 3: **SF5dB**
0 = No FS increase by 5dB
1 = FS+5dB
Bit 2: **DEEMP**: De-emphasis bit
0 = De-emphasis 50μs
1 = De-emphasis 70μs
Bit 1: **AMUTE_L**: Audio mute bit
0 = Mute
1 = Mute cancelled
Bit 0: **SE_FM**: FM radio select
0 = FM radio disabled
1 = FM radio enabled

Register 05h-MSRC_SEL-Measurement Source Select Register (Write-only)

7	6	5	4	3	2	1	0
MSR_O	AFC_LVL	DIR_AFC	RST_AFC	MSS_AFCS	MSS_SD	MSS_RF16	MSS_IF

Bit 7 **MSR_O**: Outputs VCO of IF,SD, and RF frequencies to the data pin (for testing)
- 0 = No output
- 1 = Output (for testing)

Bit 6 **AFC_LVL**: AFC trigger level
- 0 = AFC is always active
- 1 = AFC is only active when field strength is above 20dBμV

Bit 5 **DIR_AFC**: AFC operation direction
- 0 = AFC reverse operation (for testing)
- 1 = AFC normal operation

Bit 4 **RST_AFC**: AFC reset
- 0 = Normal operation
- 1 = Resets AFC to the center of control range

Bit 3 **MSS_AFCS**: Detects the AFC status by the data line
- 0 = AFC status read disabled
- 1 = AFC status read enabled

With this bit set to "1" and with MSR_O = 1, the state outside the AFC control range can be detected from the change of the DATA line.

In case of the state outside the AFC control range, the DATA line changes from L to H.

Bit 2 **MSS_SD**: Stereo decoder oscillator measurement
- 0 = Disable stereo decoder oscillator measurement
- 1 = Enable stereo decoder oscillator measurement

Bit 1 **MSS_RF16**: RF/16 measurement
- 0 = RF/16 oscillator measurement disabled
- 1 = RF/16 oscillator measurement enabled

Bit 0 **MSS_IF**: IF oscillator measurement
- 0 = Disable IF oscillator measurement
- 1 = Enable IF oscillator measurement

Note: Be sure that only one of MSS_XX bits is enabled.
The FM RF frequency is divided to 1/16 and input into the measuring circuit.

Register 06h-CTRL_STAT-Control Status Register (Read-only)

7	6	5	4	3	2	1	0
REV3	REV2	REV1	REV0	AFC_UP	AFC_DN	COV_FLG	AFC_FLG

Bit 7-4 **REV[3:0]**: 0Fh

Bit 3 **AFC_UP**: AFC adjustment up-direction
- 0 = Center value
- 1 = RF frequency adjusted in the up-direction

Bit 2 **AFC_DN**: AFC adjustment down-direction
- 0 = Center value
- 1 = RF frequency adjusted in the down-direction

Bit 1 **COV_FLG**: Counter overflow flag
- 0 = No overflow
- 1= Counter overflow

Bit 0 **AFC_FLG**: AFC out of range bit
- 0 =AFC is within control range
- 1 =AFC is out of control range

Note: COV_FLG is cleared when CLR_CNT1 bit of CNT_CTRL register is set to "1."

Register 07h – RADIO_STAT – Radio Station Status Register (Read-only)

7	6	5	4	3	2	1	0
RSS_MS	RSS_FS						

Bit 7 **RSS_MS**: mono/stereo determination
- 0 = mono
- 1 = stereo

Bit 6-0 **RSS_FS[6:0]**: Field Strength bit
- 1111111b = Field Strength<10dBμV
- 0111111b = Field Strength 10 to 20dBμV
- 0011111b = Field Strength 20 to 30dBμV
- 0001111b = Field Strength 30 to 40dBμV
- 0000111b = Field Strength 40 to 50dBμV
- 0000011b = Field Strength 50 to 60dBμV
- 0000001b = Field Strength>70dBμV

Note: +5dB for Register 04h bit3 = 1

Register 08h-STEREO_CTRL-Stereo Control Register (Write-only)

7	6	5	4	3	2	1	0
PICMPS	SD_PM	ST_M	FRCST	IF_PM_L	DCFB_SPD	DCFB_OFF	AGCSP

Bit 7 **PICMPS**: Pilot compensation
- 0 = Disable
- 1 = Enable

Bit 6 **SD_PM**: Stereo Decorder PLL Mute
- 0 = PLL ON (for normal operation)
- 1 = PLL OFF (for measurement, etc.)

Bit 5 **ST_M**: mono/stereo changeover
- 0 = Stereo
- 1 = mono

Bit 4 **FRCST**: Forced stereo
- 0 = Normal
- 1 = Forced stereo (for testing)

Bit 3 **IF_PM_L**:IF PLL Mute
- 0 = PLL OFF (for measurement)
- 1 = PLL ON (for normal operation)

Bit 2 **DCFB_SPD**: DC feedback speed
- 0 = Normal speed (for normal operation)
- 1 = High speed (for testing)

Bit 1 **DCFB_OFF**: DC Feedback control
- Fixed at 0

Bit 0 **AGCSP**: AGC speed control
- 0 = Normal speed
- 1 = High speed

Note: With this bit ON, rise of the Field strength becomes faster.

Register 09h-FM_CAP-FM RF Capacitor Bank Register (Write-only)

7	6	5	4	3	2	1	0
FMCAP[7:0]							

Bit 7-0 **FMCAP[7:0]**: FM RF frequency CAP bank (rough adjustment)

Register 0Ah-PW_SCTRL-Power and Soft Control Register (Write-only)

7	6	5	4	3	2	1	0
SS_CTRL			SM_CTRL			EXTCLK	PW_RAD

Bit 7-5 **SS_CTRL**: Soft stereo control
- 000b = Soft stereo level 3
- 001b = Soft stereo off
- 010b = Soft stereo level 1
- 100b = Soft stereo level 2

Bit 4-2 **SM_CTRL**: Soft mute control
- 000b = Soft mute level 3
- 001b = Soft mute off
- 010b = Soft mute level 1
- 100b = Soft mute level 2

Bit 1 **EXTCLK**: External clock type
- 0 = Crystal
- 1 = Oscillator

Bit 0 **PW_RAD**: Radio power
- 0 = Radio OFF
- 1 = Radio ON

Register 0Bh-SD_OSC-Stereo Decoder Oscillator Register (Write-only)

7	6	5	4	3	2	1	0
SDOSC[7:0]							

Bit 7-0 **SDOSC[7:0]**: Stereo Decoder oscillator DAC

Register 0Ch-CNT_CTRL-Counters Control Register (Write-only)

7	6	5	4	3	2	1	0
CNT1_CLR	CTAB2	CTAB1	CTAB0	SWP_CNT_L	CNT_EN	CNT_SEL	CNT_SET

Bit 7 **CNT1_CLR**: Clears the counter1
- 0 = Normal mode
- 1 = Clears the counter1

Bit 6-4 **CTAB[2:0]**: Sets the counter2 TAB value
- 000b Stop after 2 counts
- 001b Stop after 8 counts
- 010b Stop after 32 counts
- 011b Stop after 128 counts
- 100b Stop after 512 counts
- 101b Stop after 2048 counts
- 110b Stop after 8192 counts
- 111b Stop after 32768 counts

Bit 3 **SWP_CNT**: Counter swap control (0 for swap)
- 0 = Clock source 1 to counter 2, clock source 2 to counter 1 (swapping)
- 1 = Clock source 1 to counter 1, clock source 2 to counter 2 (no swap)

Bit 2 **CNT_EN**: Count start
- 0 = Count stop
- 1 = Count start

Bit 1 **CNT_SEL**: Counter select
- 0 = Counter1 used for measurement
- 1 = Counter2 used for measurement

Bit 0 **CNT_SET**: Set counters bit
- 0 = Normal mode
- 1 = Set both counter 1 and counter 2 to FFFFh and keep them set

Register 0Dh-CNT_STAT-Counters Status Register (Read-only)

7	6	5	4	3	2	1	0
Reserved	CNT_RDY	Reserved					

Bit 7 **Reserved**: 1

Bit 6 **CNT_RDY**: Count over flag
- 0 = Counting
- 1 = Count over

Note: CNT_RDY is cleared by setting the CLR_CNT 1 bit of CNT_CTRL register to"1."

Bit 5-0 Reserved: 0

Register 0Eh-IF_OSC-IF Oscillator Register (Write-only)

7	6	5	4	3	2	1	0
IFOSC[7:0]							
Bit 7-0	**IFOSC[7:0]**: IF oscillator DAC						

Register 0Fh-IF_BW-IF Bandwidth Register (Write-only)

7	6	5	4	3	2	1	0
IFBW[7:0]							
Bit 7-0	**IFBW[7:0]**: IF band width						

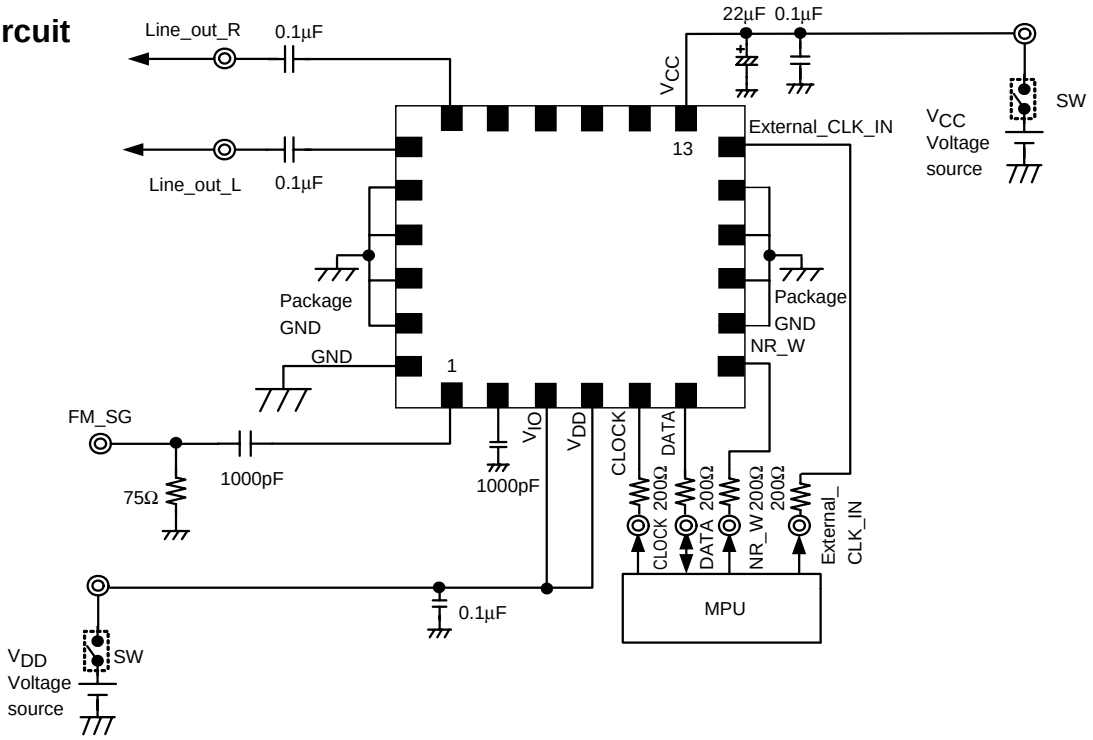
Register 10h-RADIO_CTRL1-Radio Control 1 Register (Write-only)

7	6	5	4	3	2	1	0
VREF2	VREF	STABI_BP	EN_MEAS	EN_AFC	AGC_SLVL[1:0]		AFC_SPD
Bit 7	**VREF2**: VREF2 control bit						
	0 = VREF2 is ON						
	1 = VREF2 is OFF						
Bit 6	**VREF**: VREF control bit						
	0 = VREF is ON						
	1 = VREF is OFF						
Bit 5	**STABI_BP**: Voltage stabilizer (regulator) control						
	0 = Internal voltage is Vstabi (normal operation)						
	1 = Internal voltage is V_{CC} (stabi bypassed)						
Bit 4	**EN_MEAS**: Measurement mode						
	0 = Normal mode						
	1 = Measurement mode						
Bit 3	**EN_AFC**: AFC control						
	0 = AFC OFF						
	1 = AFC ON						
Bit 2-1	**AGC_SLVL[1:0]**: AGC set level						
	Default = 0						
Bit 0	**AFC_SPD**: AFC speed control						
	0 = AFC speed 3Hz						
	1 = AFC speed 8kHz (for testing)						

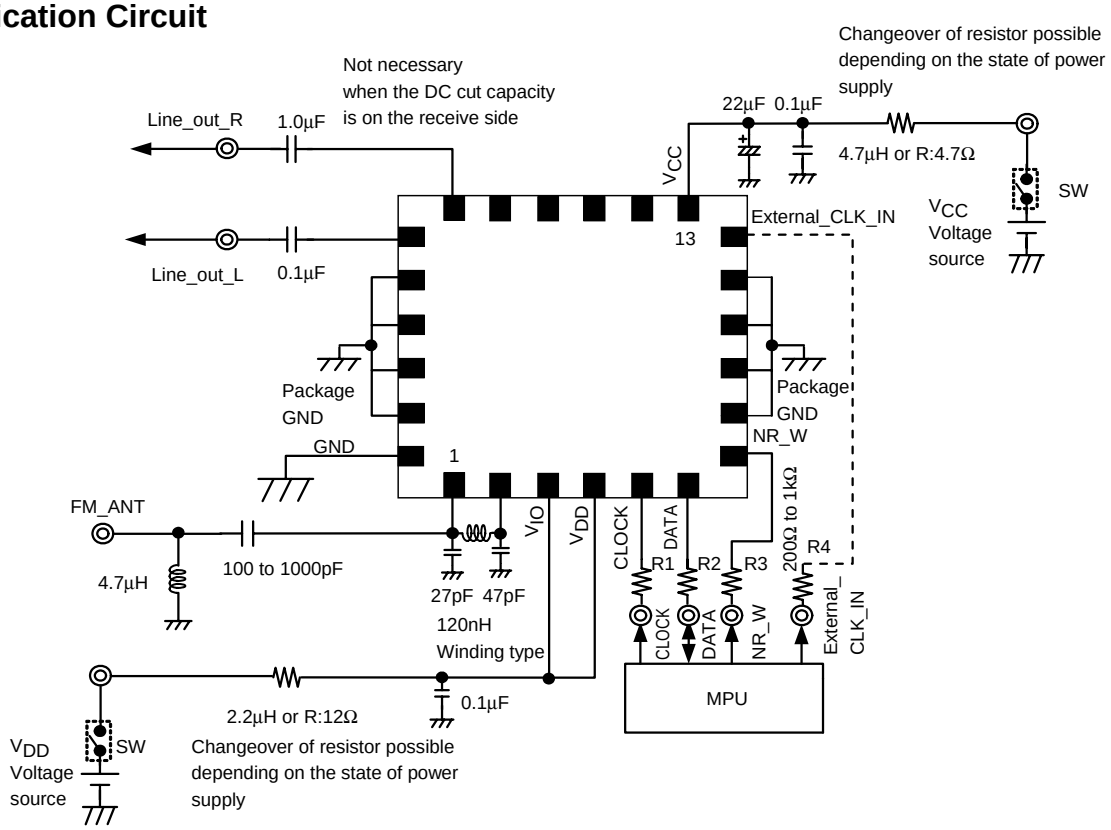
Register 11h-CNT_H-Counter Value High Register (Read-only)

7	6	5	4	3	2	1	0
CNT_MSB[7:0]							
Bit 7-0	**CNT_MSB[7:0]**: Upper 8-bit value of the 16 bit counter						

Test Circuit



Application Circuit



Note1: Vale of Extenal Component is just reference. Please set most sutable value under Acutual_ operation.

Note2: Please take Consideration of most suitable_value, as for antenna application

Note3: We recomend to put R1,R2,R3,R4 for interface between MPU and IC.

Note4: Please put Capacitor Between V_{DD} and GND also, put Capacitor Between V_{CC} and GND as shown on application.

Note5: As for AFC pin (16 pin), usually it is recommended not to connect anything. AFC can be operated more smoothly by putting capacitor between 16 pin and GND.

- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of January, 2008. Specifications and information herein are subject to change without notice.